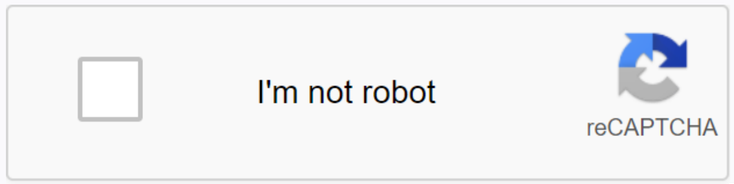

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Psk modulation pdf

The third basic digital modulation technique, and the most widely used in one form or another, is PSK. Its simplest form is Binary Phase-Shift Keying (BPSK). In BPSK, 0 and 1 are represented by different sinusoid segments in their phases. In recipients, distinguishing between the two segments is easier if their phases differ as much as possible. In BPSK the phase is separated by half a cycle (equivalent to π or 180°). See Figure 1.5. BPSK-modulated signals are less susceptible to certain types of noise than ASK. Figure 1.6 shows three examples of digitally modulated waveforms. For each example, decide which modulation scheme to use and, based on the numbers you've seen before, find out what binary data each of these represents. Figure 1.6 Three digitally modulated waveforms. Waveform (a) is an example of a BPSK-modulated waveform that represents data:0 0 0 1 0 1 1 1.Waveform (b) is an example of a BASK modulation waveform that represents data:0 0 0 0 1 1 0 1.Waveform (c) is an example of a BFSK modulation waveform representing data:1 1 0 0 1 0 1.This interactive activity will allow you to explore three binary digital modulation schemes: OOK, ASK, BFSK and BPSK. Start the activity by clicking the image or 'View' link below. You'll notice that you're invited to 'Create binary data stream'. Enter a series of 0 and 1, then click 'Submit' to create a modulation waveform and use this to modulate the operator using one of the modulation schemes. You can change the modulation scheme using the drop-down menu in the top left, and change the operator frequency using the slider in the top right. Try creating a different modulated waveform. Digital phase modulation is a versatile and widely used digital data transfer method. On the previous page, we saw that we could use discrete variations in amplitude or frequency operators as a way of representing that and zero. It should come as no surprise that we can also represent digital data using phases; this technique is called phase shift keying (PSK). Binary Phase Shift Keying Psk type is most easily called binary phase shift keying (BPSK), where binary refers to the use of two phase offsets (one for high logic, one for low logic). We can intuitively recognize that the system will be stronger if there is a greater separation between these two phases—of course it will be difficult for the receiver to distinguish between the symbol with the 90° phase offset and the symbol with the 91° phase offset. We only have 360° phases to work with, so the maximum difference between high-logic and low-logic phases is 180°. But we know that shifting a sinusoid by 180° is the same as reversing it; thus, we can think of BPSK as simply reversing the carrier in response to one state of and leave it alone in response to other logical circumstances. To go further, we know that multiplying sinusoids with negatives is the same as reversing reversing This leads to the possibility of bpsk deployment using the following basic hardware configurations: However, this scheme can easily result in a high tilt transition in the form of operator waves: if the transition between logical states occurs when the operator is at its maximum value, the operator voltage must quickly move to the minimum voltage. High slope events like this are not desirable because they produce higher frequency energy that can interfere with other RF signals. In addition, amplifiers have limited ability to produce high tilt changes in output voltage. If we improve the above implementation with two additional features, we can ensure a smooth transition between symbols. First, we need to make sure that the digital bit period equals one or more complete operator cycles. Second, we need to synchronize the digital transition with the waveform operator. With this upgrade, we can design the system in such a way that a phase change of 180° occurs when the carrier signal is at (or very close to) junction zero. QPSK BPSK transfers one bit per symbol, which is what we're used to doing so far. Everything we have discussed with respect to digital modulation has assumed that the carrier signal is modified according to whether the digital voltage is low logic or high logic, and the receiver builds digital data by interpreting each symbol as 0 or 1. Before we discuss quadrature phase shift keying (QPSK), we need to introduce the following important concept: There is no reason why one symbol can only transfer one bit. It is true that the world of digital electronics is built around circuits where the voltage is at one extreme or the other, so the voltage always represents one bit digital. But RF is not digital; instead, we use analog waveforms to transfer digital data, and it is perfectly acceptable to design systems where analog waveforms are encoded and interpreted in a way that allows one symbol to represent two (or more) bits. QPSK is a modulation scheme that allows a single symbol to transfer two bits of data. There are four possible two-bit numbers (00, 01, 10, 11), and as a result we need four offset phases. Again, we want the maximum separation between phase options, which in this case is 90°. The advantage is the higher data level: if we maintain the same symbol period, we can double the rate at which the data is moved from the transmitter to the receiver. The downside is the complexity of the system. (You may think that QPSK is also significantly more susceptible to bit errors than CPM, as there is less separation between possible phase values. This is a reasonable assumption, but if you go through the math it turns out the probability of an error is actually very similar.) The QPSK variant is, overall, effective modulation scheme. But it can be improved. The QPSK Standard Jumps phase guarantees that the symbol-to-symbol transition to the high slope symbol will occur; because phase jumps can ± 90°, we cannot use the described approach to phase jumps generated by BPSK modulation. This issue can be mitigated by using one of the two QPSK variants. The QPSK offset, which involves adding delays to one of the two digital data streams used in the modulation process, reduces the maximum phase jump to 90°. Another option is π/4-QPSK, which reduces the maximum phase jump to 135°. Thus, QPSK offsets are superior with respect to phase termination reduction, but π/4-QPSK is profitable because it is compatible with differential encoding (discussed in the next subsection). Another way to handle symbol-to-symbol termination is to implement additional signal processing that creates a smoother transition between symbols. This approach is incorporated into a modulation scheme called minimum shift keying (MSK), and there is also an improvement in MSK known as MSK Gaussian. Another difficulty coding differential is that demodulation with PSK waveforms is more difficult than with FSK waveforms. Absolute frequency in the sense that frequency changes can always be interpreted by analyzing signal variations with respect to time. The phase, however, is relative in the sense that it has no universal reference—the transmitter generates phase variations by referring to the point of time, and the receiver can interpret the phase variation by referring to a separate point in time. Practical manifestations of this are as follows: If there is a difference between phase (or frequency) oscillators used for modulation and demodulation, PSK becomes unreliable. And we have to assume that there will be phase differences (unless the receiver combines circuit recovery operators). Differential QPSK (DQPSK) is a variant that is compatible with uns inherent receivers (that is, receivers that do not synchronize demodulation oscillators with modulation oscillators). The QPSK differential encodes the data by generating a specific phase shift relative to the previous symbol. Using the previous symbol phase in this way, the demodulation circuit analyzes the symbol phase using references common to receivers and transmitters. Binary phase shift keying summary is a direct modulation scheme that can transfer one bit per symbol. Key quadrature phase shifts are more complex but double the data rate (or achieve a data rate equal to half the bandwidth). QPSK offsets, π/4-QPSK, and minimum shift keying are modulation schemes that reduce the effect of changes in symbol-to-symbol voltage to high symbols. The QPSK differential uses phase differences between adjacent symbols to avoid problems related to the lack of phase synchronization between the transmitter and receiver. Frequency-shift keying (FSK) and phase-shift keying (PSK) modulation schemes are used in digital communications, radar, RFID, and many other applications. The simplest form of FSK uses two frequencies to transmit binary information, with Logic 1 representing the frequency of the sign and Logic 0 0 frequency of space. The simplest form of PSK is binary (BPSK), which uses two phases separated by 180°. Figure 1 describes two types of modulation. Figure 1. FSK Binary Modulation (a) and PSK (b). The modulated output of direct digital synthesizers (DDS) can switch frequencies and/or phases in a phase-continuous or phase-coherent way, as shown in Figure 1, and as described in the DDS Multichannel Enables Phase-Coherent FSK Modulation, making DDS technology perfect for FSK and PSK modulation. This article describes how two synchronized DDS channels can implement FSK or PSK modulators without crossing. Here, ad9958 two-channel, 500-MSPS, full DDS (see Attachments) is used to switch frequencies or phases at zero junction points, but a synchronized two-channel solution should be able to achieve this functionality. In a phase-coherent radar system, zero-crossing switching reduces the amount of postal processing required for the introduction of target signatures; and applying PSK at zero junction reduces spectral splashing. Although both DDS-channel AD9958 outputs are independent, they share an internal system clock and are on one silicone section, so they must provide more reliable channel-to-channel tracking of temperature and power supply deviations than the output of multiple single channel devices synchronized together. The process variability that may exist between different devices is also greater than any process variability you might see between two channels created in a single piece of silicon, making multichannel DDS preferable to use as a zero-crossing FSK or PSK modulator. Figure 2. Setup for FSK or PSK modulators without crossings. An important element of DDS is the phase accumulator, which, in this implementation, is 32 bit wide. When the accumulator overflows, it maintains an excess value. When the accumulator overflows without residuals (see Figure 3), the output is right in Phase 0, and the DDS engine starts from its place at Moment 0. The rate at which zero-overflow is experienced is referred to as the DDS large recurrence rate (GRR). Figure 3. Basic DDS with overflow accumulators. GRR is determined by the far right nonzero bit of the DDS frequency adjustment word (FTW), as defined by the following equation: GRR=FS/2n where: FS is the sampling frequency of DDS. n is the far right nonzero bit of FTW. For example, DDS with a sampling frequency of 1 GHz uses FTW marks and 32-bit spaces with binary values displayed. In this case, the far right nonzero bit of one of the FTW is the 19th bit, so GRR = 1 GHz

/ 219, or about 1907 Hz. Mark (CH0) 00101010 00100110 10100000 0000 0000 Space (CH0) 001101010 1110011 1100000000 00000000 GRR (CH1) 000000000 00000000 00100000000 A DDS inherently switches frequencies gradually. This means that no instantaneous phase changes occur the frequency adjustment word changes. That is, that is, start collecting new FTW from whatever phase position it is when the new FTW is implemented. Phase coherence, on the other hand, requires an instantaneous transition to a new frequency phase as if a new frequency had been present all along. Therefore, in order for the standard DDS to implement a phase-coherent FSK switch, changes from the frequency of the sign to the frequency of space must occur when both frequencies have the same absolute phase. To implement a phase-coherent no-crossing switch, DDS must transition the frequency at 0 degrees (that is, when the accumulator overflows with zero excess). Therefore, we must determine the instance in which the zero-crossing coherent phase occurs. If the GRR mark and FTW space are known, the smaller of the two GRR (if different) will indicate the desired phase coherent zero junction point. Three criteria are required to implement a phase-coherent zero crossing switch: The ability to determine the GRR is smaller than the FTW mark and space associated with CH0 from Figure 2. The second DDS channel (CH1 of Figure 2) is synchronized to CH0 from Figure 2 and programmed with FTW which has all zeros except for one bit corresponding to the smaller GRR. Ability to use the second channel rollover to trigger frequency changes in CH0 from Figure 2. Unfortunately, the latency between when the DDS accumulator reaches zero and when phase zero is represented on the output further complicates the solution. Fortunately, this latency is constant. The ideal solution requires additional channels to be adjusted to compensate for this latency. Both channels in AD9958 have phase-offset words that can be used to fix this issue. DDS's two AD9958 channels produce the results shown in Figure 4, Figure 5, and Figure 6. Figure 4 and Figure 5 exhibit phase-continuous FSK switching vs zero-crossing FSK switching. Figure 5 shows the continuous phase transition and the coherent transition phase. Figure 6 shows the results of a pseudorandom sequence (PRS) data stream that switches between multiple frequencies. Figure 4. Continuous phase-phase FSK transition. Figure 5. FSK transition without intersection. Figure 6. Zero-crossing with multi-FSK transition. DDS's two AD9958 channels produce the results shown in Figure 7 and Figure 8. These figures show continuous phase-phase BPSK switching vs. zero-crossing BPSK redirection. Figure 7. BpSK transition is a continuous phase. Figure 8. BPSK transition is zero intersection. The Two Channel Attachment, 10-Bit, 500-MSPS Ad9958 Direct Digital Synthesizer two-channel direct digital synthesizer (DDS) comes with two 10-bit, 500-MSPS current output DAC, as shown in Figure 9. Both channels share a common system clock, providing inherent synchronization; Additional packages can be used if more than two channels are required. The frequency, phase, and amplitude of each channel can be independently controlled, so that Mismatch. These parameters can be swept linearly; or 16 levels can be selected for FSK, PSK, or ASK modulation. Output sine waves can be adjusted with 32-bit frequency resolution, 14-bit phase resolution, and 10-bit amplitude resolution. Operating with a core supply of 1.8-V, plus a 3.3-V I/O supply for logic compatibility, AD9958 consumes 315 mW with all channels on, and 13 mW in power-down mode. Determined from –40°C to +85°C, available in a 56-lead LFCSP package and priced at $20.24 in the 1000s. Figure 9. AD9958 block diagram. Diagram.